

JPW 2183

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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10/010,395	
	Filing Date	November 5, 2001	
	First Named Inventor	Devadatta V. BODAS	
	Art Unit	2183	
	Examiner Name	TBA	
Total Number of Pages in This Submission	12	Attorney Docket Number	Intel 2207/12611

ENCLOSURES (Check all that apply)		
<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment/Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input checked="" type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Response to Missing Parts/Incomplete Application <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation <input type="checkbox"/> Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____	<input type="checkbox"/> After Allowance communication to Group <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Other Enclosure(s) (please Identify below): 1. PTO-1449 and 7 references 2. International Search Report
<div>Remarks</div>		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual name	Stephen T. Neal - (Reg. No. 47,815) Attorneys for Intel Corporation
Signature	<i>Stephen T. Neal</i>
Date	May 27, 2004

CERTIFICATE OF TRANSMISSION/MAILING			
I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below. M/S: DD			
Typed or printed name	Barbara Vance	51091v1	
Signature	<i>Barbara Vance</i>	Date	May 27, 2004

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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PATENT



Docket No. 2207/12611
Assignee: Intel Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS : Devadatta V. BODAS
SERIAL NO. : 10/010,395
FILED : November 5, 2001
FOR : METHOD AND APPARATUS FOR REGULATION OF
ELECTRICAL COMPONENT TEMPERATURE AND
POWER CONSUMPTION RATE THROUGH BUS WIDTH
RECONFIGURATION
GROUP ART UNIT : 2183
EXAMINER : TBA

M/S: DD
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Date: May 27, 2004	Signature <u>Barbara Vance</u>
Barbara Vance	

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the seven (7) reference(s) listed on the attached PTO-1449 (modified) form. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

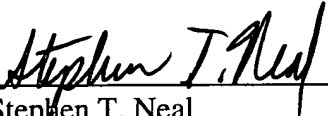
The information disclosure statement, along with the International Search Report, is being submitted under 37 C.F.R. §1.97(c)(1). I hereby certify that each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this information disclosure statement.

If any fee is required, please charge Kenyon & Kenyon, Deposit Account No. **11-0600**.

Respectfully submitted,

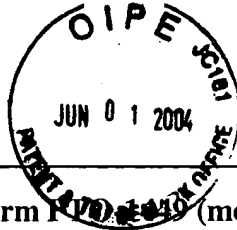
KENYON & KENYON

Dated: May 27, 2004

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Form PTO 1449 (modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT(S)' INFORMATION DISCLOSURE STATEMENT	Attorney Docket No. Intel 2207/12611	Serial No. 10/010,395
	Applicant Devadatta V. BODAS	
	Filing Date November 5, 2001	Group Art Unit 2183

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,761,456	June 2, 1998	Titus et al.	395	307	April 3, 1996
	5,936,953	August 10, 1999	Simmons	370	364	December 18, 1997
	6,304,930	October 16, 2001	Yamauchi	710	106	January 19, 1999

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	WO 00/58847	5 October 2000	WIPO	G06F	13/40	X	

OTHER DOCUMENTS

EXAMINER INITIAL	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Luca Benini, Bologna, Italy; Giovanni DeMicheli, Stanford, CA, "System-Level Power Optimization: Techniques and Tools", 1999 International Symposium on Low Power Electronics and Design, (ISLPED), San Diego, CA., AUG. 16-17, 1999. International Symposium on Low Power Electronics and Design, New York, NY, ACM, 16 August 1999 (1999-08-16), 1-58113-133-X/99/0008, pages 288-293
	L. Benini, Bologna, Italy; A. Bogliolo; G. DeMicheli, Stanford, CA, "System-Level Dynamic Power Management", Low-Power Design, 1999, Proceedings, IEEE Alessandro Volta Memorial Workshop on Como, Italy 4-5 March 1999, Los Alamitos, CA, USA, IEEE Comput. Soc., US, 4 March 1999 (1999-03-04), pages 23-31.
	"Advanced Configuration and Power Interface Specification", Advanced Configuration and Power Interface Specification, XX, XX, Pages I-XII, 1-266.

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	